DesignWare

minPower Components

Documentation Overview

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DesignWare minPower Components Documentation Overview

DesignWare minPower Components comprise a low power, technology-independent, microarchitecture-level library that is tightly integrated into the Synopsys synthesis environment.

The following sections list the documentation set and datasheets that support this library:

1.1 DesignWare minPower Components Document List

Table 1-1 DesignWare minPower Components Documentation

DesignWare minPower Components Release Notes manuals/minpower_relnotes.pdf	Contains usage issues for DesignWare minPower Components Library (F-2011.09) for Design Compiler 201109.0.
DesignWare minPower Components User Guide manuals/minpower_userguide.pdf	Explains the use of DesignWare minPower Components. NOTE: The *DesignWare minPower Application Notes* document is now Appendix A of this User Guide.
DesignWare IP Family Reference Guide https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dw_frg.pdf	Provides general information for most DesignWare Synthesizable and Verification IP.
DesignWare Building Block Quick Reference https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dwbb_qrg.pdf	Provides a brief pin and parameter descriptions for all the DesignWare minPower Components in a single document.
DesignWare minPower Components Overview datasheets/minpower_overview.pdf	Describes the Basic Library components, which provide basic implementations of common arithmetic functions that can be referenced by HDL operators in your VHDL or Verilog source code.

1.1.1 List of DesignWare minPower Components

The following table provides links to each datasheet. New IP (2010.12 and later) are indicated with a New label.

Table 1-2 List of DesignWare minPower Components

IP	Description
minPower Pipeined Floating Point Components (Overview)	
DW_lp_piped_fp_add	Low Power Pipelined Floating Point Adder (Enhanced)
DW_lp_piped_fp_div	Low Power Pipelined Floating Point Divide
DW_lp_piped_fp_mult	Low Power Pipelined Floating Point Multiplier
DW_lp_piped_fp_recip	Low Power Pipelined Floating Point Reciprocal
DW_lp_piped_fp_sum3	Low Power Pipelined 3-input Floating Point Adder
minPower Components with Datapath Gating (Overview)	
DW_fp_add_DG	Low Power Point Adder with Datapath Gating
DW_fp_addsub_DG	Low Power Floating Point Adder/Subtractor with Datapath Gating
DW_fp_cmp_DG	Low Power Floating Point Comparator with Datapath Gating
DW_fp_div_DG	Low Power Floating Point Divide with Datapath Gating
DW_fp_mac_DG	Low Power Floating Point Multiply-and-Add with Datapath Gating
DW_fp_mult_DG	Low Power Floating Point Multiplier with Datapath Gating
DW_lp_fp_multifunc_DG	Low Power Floating Point Multi-Function Unit with Datapath Gating (New)
DW_lp_multifunc_DG	Low Power Multi-Function Unit with Datapath Gating (New)
DW_fp_recip_DG	Low Power Floating Point Reciprocal with Datapath Gating
DW_fp_sub_DG	Low Power Floating Point Subtractor with Datapath Gating
DW_fp_sum3_DG	Low Power 3-input Floating Point Adder with Datapath Gating
minPower FIFO Controllers (Overview)	
DW_lp_fifoctl_1c_df	Low Power Single-clock FIFO Controller with Dynamic Flags
minPower Arithmetic Components (Overview)	
DW_lp_cntr_up_df	Low Power “Up” Counter with Dynamic Terminal Count Flag (New)
DW_lp_cntr_updn_df	Low Power “Up/Down” Counter with Dynamic Terminal Count Flag (New)
DW_lp_multifunc	Low Power Fixed-Point Multi-Function Unit
DW_lp_fp_multifunc	Low Power Floating-Point Multi-Function Unit
DW_lp_pipe_mgr	Low Power Pipeline Manager
DW_lp_piped_div	Low Power Pipelined Divider
DW_lp_piped_ecc	Low Power Pipelined Error Correction Code (ECC)

Table 1-2 List of DesignWare minPower Components (Continued)

IP	Description
DW_lp_piped_mult	Low Power Pipelined Multiplier
DW_lp_piped_prod_sum	Low Power Pipelined Sum of Products
DW_lp_piped_sqrt	Low Power Pipelined Square Root

1.1.2 List of minPower Enhanced Library Components

The following table provides links to Low Power Library datasheets. These existing components use the minPower license (DesignWare-LP) to enable low power features. New IP are indicated with a New label.

Table 1-3 List of DesignWare minPower Components

IP	Description
Enhanced pre-existing IP that have enhanced Clock Gating	
DW03_bictr_dcnto	Up/Down Binary Counter with Dynamic Count-to Flag (Enhanced)
DW03_bictr_scnto	Up/Down Binary Counter with Static Count-to Flag (Enhanced)
DW_arb_dp	Arbiter with Dynamic Priority Scheme (Enhanced)
DW_arb_sp	Arbiter with Static Priority Scheme (Enhanced)
DW_fifoctl_s1_df	Synchronous Single-clock FIFO Controller with Dynamic Flags
DW_asymfifoctl_s1_df	Asymmetric I/O Synchronous Single-clock FIFO Controller - Dynamic Flags
DW_fifoctl_s1_sf	Synchronous Single-clock FIFO Controller with Static Flags
DW_asymfifoctl_s1_sf	Asymmetric I/O Synchronous Single-clock FIFO Controller - Static Flags
DW_fifoctl_s2_sf	Synchronous Dual-clock FIFO Controller with Static Flags
DW_asymfifoctl_s2_sf	Asymmetric Synchronous Dual-clock FIFO Controller - Static Flags
DW_fifoctl_2c_df	Synchronous Dual-clock FIFO Controller with Dynamic Flags
DW03_shftreg	Shift Register
DW_dpll_sd	Digital Phase Locked Loop
DW_stackctl	Synchronous (Single Clock) Stack Controller
DW_cntr_gray	Gray Code Counter
DW_mult_seq	Sequential Multiplier
DW_div_seq	Sequential Divider
DW_sqrt_seq	Sequential Square Root
Enhanced pre-existing IP that have Datapath Gating	
DW_piped_mac	Pipelined Multiplier-Accumulator
DW_8b10b_enc	8b10b Encoder
DW_8b10b_dec	8b10b Decoder

Table 1-3 List of DesignWare minPower Components

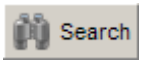
IP	Description
DW_mult_pipe	Stallable Pipelined Multiplier
DW_div_pipe	Stallable Pipelined Divider
DW_sqrt_pipe	Stallable Pipelined Square Root
DW_prod_sum_pipe	Stallable Pipelined Generalized Sum of Products
DW_mult_seq	Sequential Multiplier
DW_div_seq	Sequential Divider
DW_sqrt_seq	Sequential Square Root
DW_fp_div_seq	Floating Point Sequential Divider

1.2 Synopsys Common Licensing (SCL)

You can find general SCL information on the following page:

http://www.synopsys.com/Support/Licensing

1.3 Searching PDF Files



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1.4 Additional Information

For additional Synopsys documentation, refer to the following location:

http://www.synopsys.com/products/designware/docs

For up-to-date information about the latest verification models and synthesizable IP available from Synopsys, visit the DesignWare IP homepage:

http://www.designware.com

From this page you can “Search for IP” in the Search Tools field.